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Center for Innovative Integrated Electronic Systems
Tohoku University

World-first successful 2-Mbit STT-MRAM development with high yield and small memory cell area by applying the on-via MTJ formation technology

~ 30% area reduction and 70% yield improvement have been achieved ~

Abstract

Professor Tetsuo Endoh, Director of Center for Innovative Integrated Electronic Systems (CIES), Tohoku University, and his colleagues have successfully developed 2-Mbit Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) with high yield and small memory cell area. It has been achieved, for the first time in the world, by applying the newly developed on-via magnetic tunnel junction (MTJ) formation technology to a mega-bit class STT-MRAM, in which MTJs are stacked directly on the via holes in the Complementary Metal Oxide Semiconductor (CMOS) circuit without MTJ's characteristics degradation. The experimental result using the new 2-Mbit STT-MRAM fabricated using 90-nm CMOS and 70-nm MTJ technology on 300-mm wafers showed more than 70% bit yield improvement and 30% memory cell area reduction compared with conventional STT-MRAM. This result especially impacts on making STT-MRAM's commercialization more practical.

This successive research results that enhance a process technology to a chip integration technology stem from the CIES's specific development organization, which covers material, process, circuit, and test technologies in integrated electronic systems. CIES are improving the organization and continuing to aim at the world's leading research results by utilizing this advantageous organization.

Background

In recent CMOS memory very-large-scale-integrated-circuits (VLSIs), the increase of their power dissipation due to transistor downscaling has become more and more serious. To solve this issue, there is a method to introduce "nonvolatility", which means a function that keeps the stored data without power supply, into memory VLSIs. By this method, significant power reduction of the memory system can be achieved because no power dissipation is required for maintaining the stored data in the memory VLSIs. Many organizations including universities, research institues, and companies in the world are actively researching new memory VLSIs using various nonvolatile devices.

Among such emerging memory VLSIs, Professor Tetsuo Endoh, Director of Center for Innovative Integrated Electronic Systems (CIES), Tohoku University, and his group has been developing STT-MRAM using MTJ devices, together with developing world-highest level MTJ device itself to apply our STT-MRAM. MTJ devices have excellent features in high-speed write, low-voltage operation, high-endurance, etc., compared with the other kinds of nonvolatile devices[*1]. These features make MTJ the most promising device especially for so-called "working memory[*2]", such as dynamic random access memory (DRAM) and static random access memory (SRAM).

Research issue

To reduce the memory cell area of STT-MRAMs is a key issue for achieving low cost comparable with conventional semiconductor memories like DRAMs, and leading to commercialize STT-MRAMs. However, MTJ is a device which uses magnetism, hence the quality of the surface between MTJ and its lower electrode is also important. If the surface condition is not stable, e.g. wavy, rough, etc., the electric/magnetic characteristics of MTJ will degrade by the influence of magnetostriction and/or Villari effect[*3]. Therefore, conventional STT-MRAMs have avoided to form MTJs directly on the via hole, which is a connection device between circuits and MTJs, because the electrode surface on the via hole usually wavy by the reflection of the via hole shape. By applying such "off-via" MTJ layout, the surface condition was good enough to maintain the MTJ's characteristics, but it apparently increases the memory cell area. This conflict between the memory cell area reduction and the MTJ characteristics degradation was a serious problem that obstructs commercializing STT-MRAMs.

Past research result

Professor Tetsuo Endoh and his group in CIES, Tohoku University, has been tackled with the above conflict problem. First, the MTJ characteristic degradation formed directly on via holes was suppressed by developing a special polishing process for the the surface between MTJ and its lower electrode. This technology's effectiveness was successfully verified by the experiment using single MTJ test chips. The result was presented at International Conference on Solid State Devices and Materials (SSDM) on September, 2014 [1].

[1] S. Miura et al., *Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials (SSDM)*, Tsukuba, 2014, pp. 444-445.

Present research progress

After obtaining the above fundamental result, we designed a 2-Mbit STT-MRAM test chip using 90-nm CMOS and 70-nm MTJ technology, in order to further verify our technology's availability for the actual integrated circuits that include more than 1-million MTJs. The features of the 2-Mbit STT-MRAM test chip are as follows;

- Implementation of both the new sense amplifier circuit developed in Tohoku University and the externally-controllable reference voltage[*4] helps achieve a very high-sensitivity data read circuit for STT-MRAM. By using this data read circuit, the MR ratio[*5], which is one of the MTJ's primary parameters contributing STT-MRAM's read performance, can be around 40 % for correct read operation, while the target value of manufacturing is more than 100 %.
- Two types of memory cell layouts, one is on-via MTJ and another is off-via MTJ, are adopted in one STT-MRAM chip (each layout has 1-Mbit memory cells). By this layouts, we can compare on-via/off-via MTJ memory cell each other under the same process condition.

We fabricated the STT-MRAM test chip on 300-mm wafers, both applying and not applying our special polishing process for the lower electrodes. As a result of the experimental result using these wafers, the memory bit yield of the STT-MRAM with our new process technology improves by 70 % compared with that of the conventional STT-MRAM. Moreover, its memory cell area is reduced by 30 % because of direct on-via MTJ formation.

Significance of this research

As a result, the effectiveness of the developed on-via MTJ formation process technology has been verified even for the STT-MRAM chip having mega-bit class memory cells. This result contributes to make STT-MRAM's chip area reduced comparable to conventional DRAM, and accelerate its commercialization.

This successive research results that enhance a process technology to a chip integration technology stem from the CIES's specific development organization, which covers material, process, circuit, and test technologies in integrated electronic systems. CIES are improving the organization and continuing to aim at the world's leading research results by utilizing this advantageous organization.

This research result was presented in IEEE[*6] International Memory Workshop (IMW) held at Paris, France, on May 16, 2016.

Acknowledgment

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Terms

*1 other kinds of nonvolatile devices: There are, for example, ferroelectric device, phase-change device, electric-field-induced resistive device, etc. Using these devices, ferroelectric RAM (FeRAM), phase change RAM (PCRAM), resistive RAM (ReRAM) are produced.

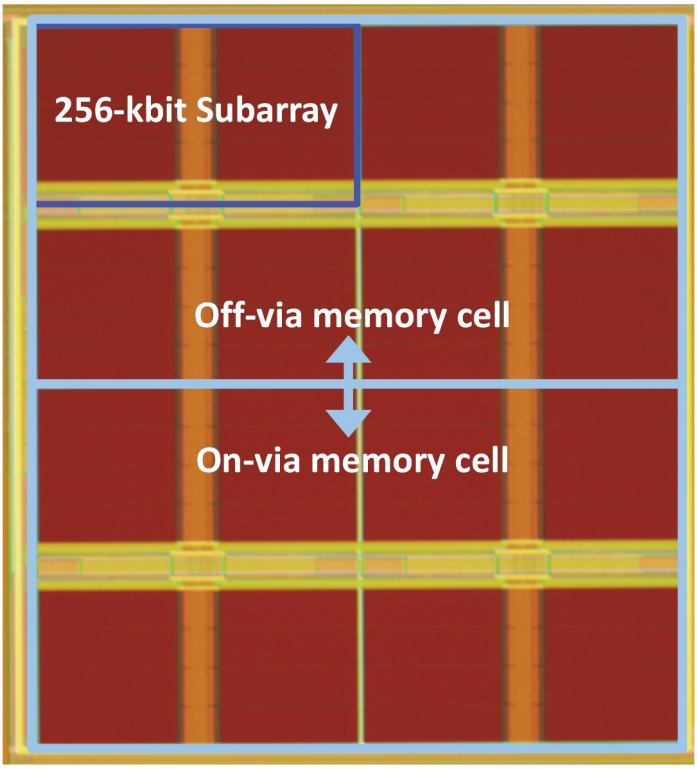
*2 working memory: memory that operates at relatively high speed (several 10 MHz to a few GHz) in memory hierarchy of computer systems. DRAM and SRAM are the representative working memories.

*3 magnetostriction, Villari effect: Magnetostriction is a property that changes the shape of a magnetic material when a magnetic field is applied. On the contrary, Villari effect is a property that changes the magnetization of a magnetic material when pressure is applied.

*4 reference voltage: It is an essential voltage for STT-MRAM's read operation. It must to be optimally controlled for correct read operation.

*5 MR ratio: It indicates (R_{ap} - R_p)/R_p in %, where R_{ap}, R_p shows the MTJ resistance for "1"-state and "0" state, respectively. The larger MR ratio means the better performance.

*6 IEEE: Abbreviation of the Institute of Electrical and Electronics Engineers, Inc. This is the largest organization in the world which is related to electric/electronic technologies.



Fabricated 2-Mbit MRAM test chip for verifying the developed MTJ formation technology directly on via holes in memory VLSI.